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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,945	09/12/2003	Neil Birkett	9931-042	8389
20575 7590 10/30/2007 MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204				
			EXAMINER VLACHOS, SOPHIA	
			ART UNIT 2611	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/661,945

Applicant(s)

BIRKETT, NEIL

Examiner

SOPHIA VLAHOS

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 9/28/2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2,4-8,10,12,13 and 26-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2,4-8,10,12,13 and 26-33 is/are rejected.
- 7) ☒ Claim(s) 2 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>10/12/2007</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claim 1 is withdrawn in view of the newly discovered reference(s) Moriwaki (U.S. 5,014,056) and Sacca (U.S. 5,680,075). Rejections based on the newly cited reference(s) follow.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 10/12/2007 has been considered by the examiner.

Specification

3. The revised abstract received on 9/28/2007 is acceptable.

Claim Objections

4. Claim 2, line 6 after the preamble reads: " produce a detected I and Q signal, the detecting comprising;" the ";" should be replaced by a semicolon. Furthermore, as recited in claims 2, the step of adjusting is interpreted (for the purpose of prior art rejections) to be responsive to the digitizing step.

Claim 26 the preamble reads "A method comprising;" where the ";" should be a semicolon.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2, 4, 10, 12 are rejected under 35 U.S.C. 103(a) as being obvious over Birkett et. al., (U.S. 6,977,976) in view of Mohindra (7,110,734) and Moriwaki (U.S. 5,014,056).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by

showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(I)(1) and § 706.02(I)(2).

With respect to claim 2, as best understood, Birkett et. al., disclose:

(a) at a specified stage in an I/Q baseband strip containing multiple automatic gain control (AGC) stages (Fig. 2, see AGC stages 29_1 through 29_n column 6, lines 47-54) , each of the AGC stages having locally generated control signals associated therewith (Fig 4a embodiment of AGC stages, column 7, lines 53-54 and Fig. 6 (the controller of Fig. 4a), column 9, lines 14-16): detecting respective I and Q output signals received from respective I and Q variable gain amplifiers (VGAs) associated with the AGC stage to produce a detected I and Q signal, the detecting comprising: (see Fig. 6 detector, receiving I and Q signals) rectifying each of the respective I and Q output signals (Fig. 6 rectifiers 62I and 62Q); adding the respective I and Q rectified filtered output signals (Fig. 6, adder 63); passing the added I and Q rectified filtered output signal through a low pass filter to produce the detected I and Q signal; (LPF) (Fig. 6, integrator 64 that functions as a low pass filter (see column 9, lines 37-39); digitizing the detected I and Q signals (see column 9, lines 55-59, see digital nature of the signals in and out of block 65 of Fig. 6); and adjusting with the associated control signal the respective I and Q VGAs for differences between the detected I and Q signal and a reference signal (Fig. 6 part of the digitizing since digitizing involves the detected signal to be compared with a reference level, see column 9, lines 39-43, and lines 56-59 where comparison in the digital domain is used, see also that the

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gain estimate is fed back to control the I and Q VGAs as shown in Fig. 4a); and (b) repeating (a) through each AGC stage (Fig 4a and Fig. 6 are understood to be applicable to all stages of the circuit shown in Fig. 2).

Birkett et. al., do not expressly teach: step passing said respective I and Q signals through respective high pass filters (HPFs); and Birkett et. al., do not expressly teach that the adder is an operational amplifier; and where the digitizing comprises receiving in an analog to digital converter (ADC) the detected I and Q signal, comparing the detected I and Q signal to the reference signal, and generating digital up/down and count/hold signal.

In the same field of endeavor (zero-IF receiver) Mohindra disclose: passing I and Q signals through respective high pass filters (HPFs) (see Fig. 1, HPFs 24 and 25 filtering I and Q signals respectively, column 2, lines 3-5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett et. al., based on the teachings of Mohindra to pass I and Q signals through respective high pass filters (HPFs) to remove (residual) DC errors.

With respect to the limitation: adding said respective I and Q filtered output signals in an operational amplifier, the combination of Birkett et. al. and Mohindra, disclose summing the I and Q filtered signals, and with respect to the specific nature of the summer (i.e. op-amp) operational amplifiers and their configurations (i.e. op-amp adders) are well known in the art. Therefore it would have been obvious to a person of ordinary skill in the art at the time of the

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invention to use an op-amp to perform addition, and use use few /cheap/widely available components to perform addition (op-amp).

Solving the same issue (conversion to digital signals), Moriwaki discloses that digitizing comprises: receiving in an analog to digital converter (ADC) an input signal (Fig. 6, see ADC circuit), comparing the input signal to the reference signal (Fig. 6 comparators 16a... 16c, comparing bit outputs corresponding to the input signal to reference voltages, column 9, lines 8-12, 33-46), and generating digital up/down and count/hold signal (see column 9, lines 3-7, and see counter 20 on Fig. 6, see also Fig. 7A, showing signals F, S, and stop-count, see column 9, lines 47-67, through column 10, lines 1-3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett et. al., based on the teachings of Moriwaki (that teaches an ADC and discloses specifics concerning its function), so that the detected I and Q signal of Birkett et. al., is digitized as taught by Moriwaki in a fast and high-resolution A/D converter (see Moriwaki , column 1, lines 8-10).

With respect to claim 4, the system obtained by the combination of Birkett, Mohindra, and Moriwaki further includes: wherein the comparing comprises using a multi-level comparator and a logic circuit to generate the digital up/down and count/hold control signal (Moriwaki see Fig. 6, and Fig 7A, see plurality of comparators 16a through 16c corresponding to the claimed multilevel comparator and the logic circuits to the right of the comparators up to the up/down counter

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correspond to the claimed logic circuit that generates the digital/up/down and count/hold control signals, column 9, lines 47-67, column 10, lines 1-15).

Apparatus claim 10 is rejected based on a rationale similar to the one used to reject method claim 2 above since claim 10 recites specific components used to implement the steps of method claim 2.

With respect to claim 12, the system obtained by the combination of Birkett, Mohindra, and Moriwaki further includes: wherein the number of levels in the multi-level comparator is at least four (see Moriwaki Fig. 7A, the levels correspond to -5V, 0V, 0.3125V, and 5V).

7. Claims 5-8, 13 are rejected under 35 U.S.C. 103(a) as being obvious over Birkett et. al., (U.S. 6,977,976) in view of Mohindra (7,110,734) Moriwaki (U.S. 5,014,056), and further in view of Sacca (U.S. 5,680,075).

With respect to claim 5, the system obtained by the combination of Birkett, Mohindra, and Moriwaki further includes: setting the gains of the respective I and Q VGAs (see Birkett et. al., Fig. 4a, output of control block 44 is supplied to VGAs, column 9, lines 48-51).

However, neither Birkett nor Mohindra and Moriwaki expressly teach: wherein the adjusting comprises: receiving in an up/down counter the digital up/down and count/hold control signals.

In the same field of endeavor (digital domain control of a VGA), Sacca discloses: wherein the adjusting comprises: receiving in an up/down counter the digital up/down and count/hold control signals (see Fig. 2A, see digitally controlled programmable gain amplifier (PGA) (Fig. 4A and Fig. 5, column 8, lines 24-31), see column 6, lines 15-20, lines 48-60, see counting function of A/D and stopping of the counter).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett, Mohindra, and Moriwaki based on the teachings of Sacca, so that the adjusting comprises: receiving in an up/down counter the digital up/down and count/hold control signals, so that an inexpensive and free of noise digital AGC system is used (Sacca, column 3, lines 1-11, 26-32).

With respect to claim 6, the system obtained by the combination of Birkett, Mohindra, Moriwaki, and Sacca further includes: of the detected I and Q signal falls outside a predefined boundary, modifying the gains of the respective I and Q VGAs until the respective I and Q output signals achieve desired magnitudes; else, maintaining the gains of the respective I and Q VGAs (see Birkett et al., column 9, lines 44-50 where the adjusted gain is within an allowable gain range, column 9, lines 45-47 and the invention relates to AGC i.e. bringing the signal levels out of the AGCs at a specified value when the input signal varies within a specific dynamic range).

With respect to claim 7, the system obtained by the combination of Birkett, Mohindra, Moriwaki and Sacca further includes: where modifying comprises adjusting the respective I and Q VGA at a fast rate if the detected I and Q signal is beyond a first predefined range (see Moriwaki Fig. 7A, the fast count-up (down) regions, where the count is generated in response to the detected input signal (i.e. the detected I and Q signal of the system of Birkett as modified by Mohindra, and Moriwaki) or at a slow range if the detected I and Q signal is beyond a second predefined range but not beyond the first predefined range (see Fig. 7A of Moriwaki, slow count-up (down) regions, and see that the FR and AR regions of Fig. 7A do not overlap).

With respect to claim 8, the system obtained by the combination of Birkett, Mohindra, Moriwaki and Sacca further includes: wherein modifying comprises adjusting the respective I and Q VGAs at a large magnitude if the detected I and Q signal is beyond a first predefined range or at a small magnitude if the detected I and Q signal is beyond a second predefined range but not beyond the first predefined range.

With respect to claim 13, claim 13 is rejected based on a rationale similar to claim 5 above.

8. Claims 20, 26, 31-33 are rejected under 35 U.S.C. 103(a) as being obvious over Birkett et. al., (U.S. 6,977,976) in view of Moriwaki (U.S. 5,014,056).

With respect to claim 20, Birkett et. al., disclose: I and Q variable gain amplifiers (VGAs) to generate I and Q signals (see Fig. 4a, see the I and Q VGAs 43I, 43Q), respectively; a detector to generate a detect signal from the I and Q signals (see Fig. 4a, control 44, see details shown in Fig. 6, column 4, lines 17-18, see signal d, detected signal, column 9, lines 14-43) convert the detect signal to a digital detect signal (see column 9, lines 56-59, digital signals used with digital circuitry); digital engine to generate a control signal responsive to the digital detect signal and a reference signal (column 9, lines 56-59, see control signal to VGAs, responsive to the digital detect signal and a reference signal (where part of digitizing involves comparison with a reference signal)); and where the I and Q VGAs operate responsive to the control signal (column 9, lines 39-44).

Birkett et. al., do not expressly teach: an analog to digital (ADC) to convert the detect signal to a digital detect signal; where the ADC is enabled to compare the detect signal to the reference signal, and generate digital up/down and count/hold control signals as the digital detect signal;

Solving the same issue (conversion to digital signals), Moriwaki discloses that digitizing comprises: an analog to digital converter (ADC) where the ADC is enabled (Fig. 6, see ADC circuit) to compare an input signal to the reference signal (Fig. 6 comparators 16a...16c, comparing bit outputs corresponding to the input signal to reference voltages, column 9, lines 8-12, 33-46), and generate digital up/down and count/hold signal as the digital detect signal(see column 9,

lines 3-7, and see counter 20 on Fig. 6, see also Fig. 7A, showing signals F, S, and stop-count, see column 9, lines 47-67, through column 10, lines 1-3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett et. al., based on the teachings of Moriwaki (that teaches an ADC and discloses specifics concerning its function), so that the detected I and Q signal of Birkett et. al., is digitized as taught by Moriwaki in a fast and high-resolution A/D converter (see Moriwaki, column 1, lines 8-10).

With respect to claim 31, the system obtained by the combination of Birkett et. al., and Moriwaki further includes: where the ADC comprises a multi-level comparator and a logic circuit; where the multi-level comparator is enabled to compare the detect signal to the reference signal; and where the logic circuit is coupled to the multi-level comparator and is enabled to generate the digital up/down and count/hold control signals (see Fig. 6 and Fig. 7a the multilevel comparator comprising the 16a-16c comparators, see also the up/down counter 20 and signals out of multilevel comparator, of Moriwaki, column 9, lines 46-67, column 10, lines 1-3).

With respect to claim 26, Birkett et. al., disclose: at each of a plurality of serially connected gain control stages (Fig. 1, see the cascaded AGC stages 14₁ through 14_n), each of the stages having a respective I variable gain amplifier with a respective I output signal and a respective Q variable gain amplifier with a

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respective Q output signal (Fig. 4a, VGAs 43I 43Q); generating a respective detect signal from the respective I and Q output signals (control 44 details are shown in Fig. 6, signal d is the detect signals, see column 4, lines 17-18, column 9, lines 14-36) ; at each of the stages, converting the respective detect signal to a respective digital detect signal (column 9, lines 53-59 where signals in the digital domain are used); at each of the stages (column 9, lines 14-36, where it is understood that the details apply to the cascaded AGC stages), generating a respective control signal to control the respective I and Q variable gain amplifiers responsive to the respective digital detect signal; at each of the stages (see column 9, lines 53-59), adjusting the respective I and Q variable gain amplifiers responsive to the respective control signal (see gain control signals, column 9, lines 53-59);

Birkett et. al., do not expressly teach: and where the converting comprises comparing the respective detect signal to a respective reference signal via a multi-level comparator and a logic circuit.

Solving the same issue (conversion to digital signals), Moriwaki discloses where the converting comprises: (Fig. 6, see ADC circuit) comparing a signal to a respective reference signal via a multi-level comparator and a logic circuit (Fig. 6 comparators 16a...16c, comparing bit outputs corresponding to the input signal to reference voltages, column 9, lines 8-12, 33-46), and generate digital up/down and count/hold signal as the digital detect signal(see column 9, lines 3-7, and see counter 20 on Fig. 6, see also Fig. 7A, showing signals F, S, and stop-count, see column 9, lines 47-67, through column 10, lines 1-3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett et. al., based on the teachings of Moriwaki so that the converting comprises: comparing the respective detect signal of Birkett et. al., to a respective reference signal via a multi-level comparator and a logic circuit as that a digital signal is obtained using a fast and high-resolution A/D converter (see Moriwaki , column 1, lines 8-10).

With respect to claim 32, the system obtained by the combination of Birkett et. al., and Moriwaki further includes: where the converting comprises generating digital up/down and count/hold control signals via the logic circuit.

With respect to claim 33, the system obtained by the combination of Birkett et. al., and Moriwaki further includes: where the generating the respective control signal comprises: (a) receiving in an up/down counter the digital up/down and count/hold control signals; and (b) determining the respective control signal based, at least in part, on the value of the up/down counter.

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being obvious over Birkett et. al., (U.S. 6,977,976) in view of Moriwaki (U.S. 5,014,056) and further in view of Liang (U.S. 7,145,934).

With respect to claim 21, neither Birkett et. al., nor Moriwaki expressly teach: I and Q buffer amplifiers between the variable gain amplifiers and the detector to buffer the I and Q signals, respectively.

In the same field of endeavor (RF receivers, Fig. 3, column 2, lines 1-2,) Liang discloses: I and Q buffer amplifiers to buffer the I and Q signals, respectively (Fig. 3, see receiving side 330, buffer and amplifiers 334, 344 for the I and Q signals, column 6, lines 34-36).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett et. al., and Moriwaki based on the teachings of Liang, so that I and Q buffer amplifiers between the variable gain amplifiers and the detector to buffer the I and Q signals, respectively, the motivation being the buffer/amplifiers are used to buffer and amplify the I and Q signals at the receiver.

10. Claims 22- 25, 27-30 are rejected under 35 U.S.C. 103(a) as being obvious over Birkett et. al.; (U.S. 6,977,976) in view of Moriwaki (U.S. 5,014,056) and further in view of Mohindra (7,110,734).

With respect to claim 22, neither Birkett et. al., nor Moriwaki expressly teach: respective I and Q high pass filters to generate I and Q filtered signals by removing direct current offsets from the I and Q signals.

In the same field of endeavor (zero-IF receiver) Mohindra disclose: passing I and Q signals through respective high pass filters (HPFs) (see Fig. 1, HPFs 24 and 25 filtering I and Q signals respectively, column 2, lines 3-5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Birkett et. al., and Moriwaki based on the

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teachings of Mohindra to pass I and Q signals through respective I and Q high pass filters (HPFs) to remove (residual) DC errors.

With respect to claim 23, the system obtained by the combination of Birkett et. al., Moriwaki, and Mohindra further includes: respective rectifiers communicating with the respective I and Q high pass filters to change each of the I and Q filtered signals from alternating current to direct current, producing I and Q rectified filtered signals (see Birkett et. al., Fig. 6, rectifiers 62I and 62Q).

With respect to claim 24, the system obtained by the combination of Birkett et. al., Moriwaki, and Mohindra further includes: the detector includes: (circuitry to) generate an added I and Q signal by adding the I and Q rectified filtered signals (see Fig. 6 of Birkett et. al., adder block 63).

The combination of Birkett et. al., Moriwaki, and Mohindra do not expressly teach that an operational amplifier (is used) to generate an add I and Q signal. Operational amplifiers and their configurations (i.e. op-amp adders) are well known in the art. Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to use an op-amp to perform addition, and use use few /cheap/widely available components to perform addition (op-amp).

With respect to claim 25, the system obtained by the combination of Birkett et. al., Moriwaki, and Mohindra further includes: the detector includes: a

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low pass filter to filter the added I and Q signals to produce the detect signal

(Birkett et. al., Fig. 6 integrator 64, column 9, lines 37-39).

Claims 27-28 are rejected based on rationale similar to the one used to reject claim 22, 23, respectively.

With respect to claim 29, the limitations of claim 29 are disclosed by the system obtained by the combination of Birkett et. al., Moriwaki, and Mohindra further includes: where the generating the respective detect signal comprises: adding the respective I and Q rectified filtered signals to produce a respective added I and Q rectified filtered signal (see Fig. 6 of Birkett et. al., adder block 63).

With respect to claim 30, claim 30 is rejected based on rationale similar to the one used to reject claim 25 above.

Contact Information


Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
10/26/2007


MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER